Analysis and design of a two-stage CMOS operational amplifier in 150 nm technology

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Abstract - This paper describes the topology of the two-stage CMOS operational amplifier, optimum performance design guidelines and the results of simulations done in Cadence Spectre simulator using the 150 nm technology. The designed operational amplifier is for low-voltage applications and achieves performance in the range of commercially available op amps such as: open loop gain of 75 dB, unity frequency of 50 MHz, 65° phase margin, 0.3 mW power dissipation for V_{DD}=1.8V, slew rate of 10V/μs, maximum settling time 150ns.

Keywords - CMOS, two-stage, operational amplifier.

I. Introduction

The current market demands for all-in-one devices have led to the development of mixed signal circuits, combining their digital processing power and analogue interface with the real world. General aim for digital circuits is making them smaller, faster and more power efficient. The power supply decreases as a direct result of CMOS scaling and at the same time this result downgrades the performance of analogue circuits. Sub-micrometer technologies, dominantly used for digital designs, create transistors in analogue designs with low output resistance. As a consequence those transistors have poor amplifying performances. Moreover, the power supply voltage decrease results in lower gate-source voltage which in turn decreases mosfet transconductance. These bottlenecks force analogue designers to run many circuit simulations to achieve targeted performance. From this came the motivation to design a low voltage two-stage operational amplifier (op amp for short) in a 150 nm (mixed signal circuit) technology and to achieve performance in the range of commercially available op amp ICs.

The two-stage CMOS op amp is a classical topology which, when carefully designed, can achieve desired performances and is often used as a benchmark for modern designs. It uses two voltage amplifiers connected in cascade to achieve high differential voltage gain. There is also an optional third stage (output buffer) but is often left out of the design if the op amp drives capacitive load. This type of op amps fall into a subcategory called operational transconductance amplifiers (OTA) [1].

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II. Topology Analysis

The first stage of a two-stage op amp is the differential amplifier while the second one is the common source amplifier, shown in Fig. 1. The differential pair is pmos type which defines second stage as nmos common source amplifier. A complementary design is also possible but the one given in Fig. 1 shows higher slew rate and lower flicker noise. However, its disadvantage is higher thermal noise. The overall voltage gains for pmos-nmos or nmos-pmos op amp stage topologies are similar and proportional to the product of the individual gain of each pmos and nmos stage (cascade connection).

There are certain geometric ratios that exist in the design to ensure minimal systematic offset and immunity to variations (supply voltage, temperature and process variations). The systematic (inherent) voltage offset can be minimized if you maintain geometric ratios shown in Eq. (1) [2].

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}. \qquad (1)$$

The transistors Q_3 and Q_4 make a current mirror. When the differential signal is zero (but there is a common mode signal to insure that Q_1 and Q_2 are turned on) the current of the transistor Q_5 splits equally into transistors Q_1 and Q_2. The current I_{D5} is also mirrored into I_{D6} and therefore there is a hidden relationship between I_{D6} and $I_{D1,2}$ that needs to be maintained. If that is not the case, due to the offset voltage and high open loop gain, the output voltage of an op amp will reach one of the supply rails.

To understand how the impact of variations is minimized it is necessary to understand how frequency compensation is gained. Small signal scheme of the op amp is shown in Fig. 2. The voltage controlled current sources represent the amplifying stages while additional passive components represent their parallel resistive and capacitive loads, expressed in Eqs. (2) to (5) [2]. The variable r_{dsi} (i=1, 2, 3…) represents the output resistance of the transistor in the small signal analysis.

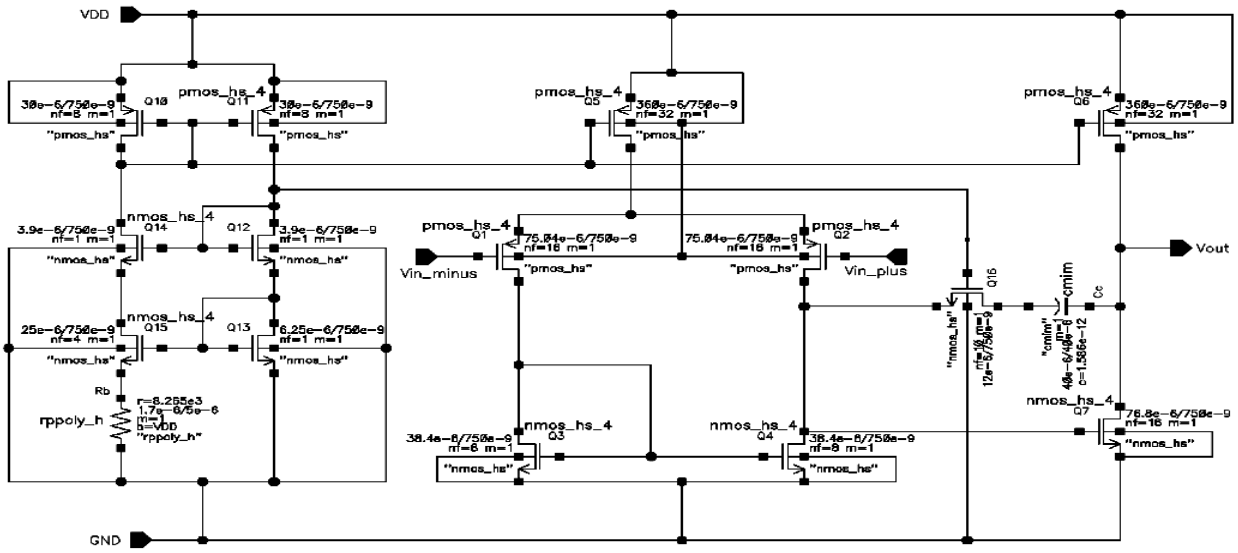

Fig. 1. Schematic of the two-stage op amp circuit.

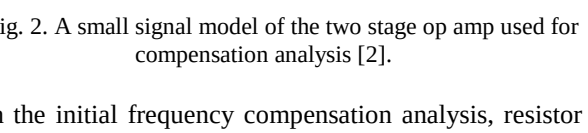

Fig. 2. A small signal model of the two stage op amp used for compensation analysis [2].

In the initial frequency compensation analysis, resistor R_C is neglected. If we solve this circuit and find the voltage gain (its transfer function) the Eq. (6) [2] is obtained. From it, the expressions for the first and second pole can be extracted, if the poles are real and the second pole is on a much higher frequency than the first pole, as show in Eqs. (9) and (10) [2].

$$R_1 = r_{ds4} \parallel r_{ds2}. \tag{2}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs7}. \tag{3}$$

$$R_2 = r_{ds6} \parallel r_{ds7}. \tag{4}$$

$$C_2 = C_{db7} + C_{db6} + C_L, \tag{5}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m7}R_1R_2(1-\frac{sC_c}{g_{m7}})}{1+a\cdot s+b\cdot s^2}, \tag{6}$$

where a and b are equal to:

$$a = (C_2 + C_c)R_2 + (C_1 + C_c)R_1 + g_{m7}R_1R_2C_c. \tag{7}$$

$$b = (C_2C_c + C_1C_c + C_1C_2)R_1R_2. \tag{8}$$

$$\omega_{p1} \approx \frac{1}{R_1[C_1 + C_c(1+g_{m7}R_2)] + R_2(C_2 + C_c)}. \tag{9}$$

$$\omega_{p2} \approx \frac{g_{m7}}{C_1 + C_2 + \frac{C_1C_2}{C_c}}. \tag{10}$$

It can be seen from the Eqs. (9) and (10) [2] that the first pole depends on $1/g_{m7}$ while the second is proportional to g_{m7}. With g_{m7} increase poles are further apart from one another which is possible due to capacitor C_C presence. The approach is commonly known as the pole splitting technique while C_C is called Miler's capacitance. There is also a zero in the right half of the complex plane which in terms of a phase shift acts like a left sided pole. This means that the zero inserts a negative 90° into the phase and makes the circuit unstable.

When R_C is introduced into the scheme (in Fig.1 it is Q_{16} polarized in deep triode region), the fundamental difference is in the position of the zero, now expressed with Eq. (11) [2]. A designer can now influence the zero position giving him a couple of options to achieve better op amp stability. The first option is to choose the value of R_C such that the zero is canceled which means its somewhere in the infinity. The second option is to put the zero around the second pole so that they can cancel each other out. This is rarely used because you can't tell in advance the value of C_2 especially in OTAs. The third option is to put the zero

slightly higher than the unity gain frequency when there is no resistor. The R_C value is then calculated with Eq. (12) [2].

$$\omega_z = -\frac{1}{C_c(1/g_{m7} - R_c)}. \quad (11)$$

$$R_C \approx \frac{1}{1.2 \cdot \omega_u C_C}. \quad (12)$$

This way we can increase the unity gain frequency by 20% and also the phase margin by approximately 40°. If R_C value is too high the gain and phase characteristics do not steadily decrease above unity-gain frequency which can distort the signal.

From the third option we can describe the design methodology for achieving a desired phase margin (PM). First, chose an initial value for the capacitor C_C e.g, 1 pF. Then write down the frequency and gain for which the phase is equal to 180° + 40° – PM (40° due to moved zero). The third step is to increase the value of C_C by multiplying it with the previously written gain value. After that the value of an actual resistor R_C can be calculated using Eq. (12) [2]. This step will require a series of iterations.

When you find adequate R_C value the final step is to replace the resistor with a mosfet in the deep triode region. The capacitor doesn't allow dc current through Q_{16} so V_{DS16} is always zero. Transistor Q_{16} dimension ratio can be approximately calculated with Eq. (13), which is result of circuit current mirrors and topology. Note that I_{D5} - corresponds to the dc current of transistor Q_5 which is copied from the polarization circuit.

$$\left(\frac{W}{L}\right)_{16} \approx \frac{1}{R_C\sqrt{2I_{D5}\mu_n C_{OX}}\sqrt{\frac{(W/L)_{10}}{(W/L)_5(W/L)_{12}}}}. \quad (13)$$

The immunity to variations is achieved with the polarization circuit and by maintaining certain geometrical ratios. This means that the position of the zero, given in Eq. (11) [2], doesn't change due to variations. If $1/g_{m7}$ decreases then R_C needs to decrease its value by the same amount so that their difference remains the same. To achieve this, the expression shown in Eq. (14) [2] has to be fulfilled.

$$\frac{(W/L)_6}{(W/L)_7} = \frac{(W/L)_{11}}{(W/L)_{13}}. \quad (14)$$

The frequency stability of the op amp and stabilized values of transconductances are achieved as a result of the polarization circuit topology and resistor R_b, shown in Fig. 1. If the dimensional ratios of Q_{10} and Q_{11} are equal the currents I_{D10} and I_{D11} will be the same. From the II KVL for the loop which consists of R_b, Q_{13} and Q_{15} dependence of g_{m13} on R_b and well defined geometry is achieved, Eq. (15) [2].

$$g_{m13} = \frac{2}{R_b}\left(1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right). \quad (15)$$

All the currents in the op amp are mirrored from the polarization circuit. If the mirroring is ideal (channel length modulation is not taken into account) and body effect is neglected, the op amp transconductances values are calculated from Eqs. (16) and (17) [2].

$$g_{miPMOS} = g_{m13} \cdot \sqrt{\frac{\mu_p}{\mu_n}\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}}. \quad (16)$$

$$g_{miNMOS} = g_{m13} \cdot \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}}. \quad (17)$$

Where i = 1, 2, 3… corresponds to the index of the transistor in Fig. 1.

III. Simulation Results

Simulations were done using the same length for all of the transistors to make current mirroring precise, by minimizing errors due to the side diffusion of the source and drain areas [3]. The length value was chosen so that the transistors behave like long channel devices with high output resistance. As a result, the impact of channel length modulation is decreased resulting in higher differential voltage gain. The optimum length was 750 nm or five times larger then the minimum value (150nm).

Transistor dimensions for the initial simulation were hand calculated to fulfill the targeted performances. Op amp design parameters (diff. gain, unity frequency, phase margin etc.), were chosen in the range of currently available commercial low-voltage op amps values. Targeted performance parameters are shown in Table I while the transistor widths, capacitor and transistor values of the final iteration are shown in Table II.

TABLE I
Targeted performance parameters

Differential gain [dB]	≥75
Unity frequency [MHz]	≥50
Phase margin [°]	≥60
Capacitive load [pF]	=3
Slewrate [V/μs]	≥2.7
Power dissipation [mW]	≤0.6
CMRR and PSRR [dB]	≥60

TABLE II
DESIGN PARAMETERS OF THE FINAL ITERATION

$W_{1,2}$	75.04 μm, Nfingers = 16
$W_{3,4}$	38.4 μm, Nfingers = 8
$W_{5,6}$	360 μm, Nfingers = 32
W_7	76.8 μm, Nfingers= 16
$W_{10,11}$	30 μm, Nfingers = 8
$W_{12,14}$	3.9 μm, Nfingers = 1
W_{13}	6.25 μm, Nfingers = 1
W_{15}	25 μm, Nfingers = 4
W_{16}	12 μm, Nfingers = 10
C_C	1.586 pF, A =40x40 μm^2
R_C	8256 Ω

Unless otherwise stated, simulation results are done for room temperature and power supply voltage of 1.8V. Analyses were conducted in the Spectre simulator. For conducting the DC and AC analysis a dc-point trick [4] was needed to insure that transistors were correctly biased. This was done with a switch whose position depends on the type of analysis that is currently running. Fig. 2 illustrates how to connect the switch. The dc generator in the feedback branch provides a different input/output dc-point by changing its dc voltage. The results of input and output common mode voltage ranges are shown in Table III and represent the range in which performances do not fall bellow 95% of the set specifications.

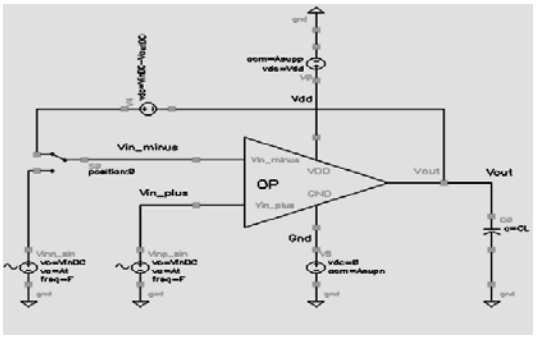

Fig. 2. Test bench circuit for the op amp.

TABLE III
COMMON MODE VOLTAGE RANGES

Parameters	From [V]	To [V]
Diff. gain > 71.25 dB (75dB – 5%)	0	1.32
Unity freq. > 47.5 MHz (50 MHZ -5%)	0	1.01
Phase margin > 57° (60° – 5%)	0	1.439
Input common mode range	0	1.01
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Diff. gain > 71.25 dB (75dB – 5%)	0.32	1.6
Unity freq. > 47.5 MHz (50 MHZ -5%)	0.10	1.34
Phase margin > 57° (60° – 5%)	0.09	1.8
Output common mode range	0.32	1.34

It is interesting to illustrate how the compensating branch works. In Fig. 3 are shown results without the capacitor C_C and transistor Q_{16}. When C_C is inserted the first pole frequency is lowered and the phase margin is increased (Fig 4). After Q_{16} is introduced into the circuit, the unity frequency and phase margin is increased as shown on Fig. 5. Both behaviors are within conclusions given in Section II.

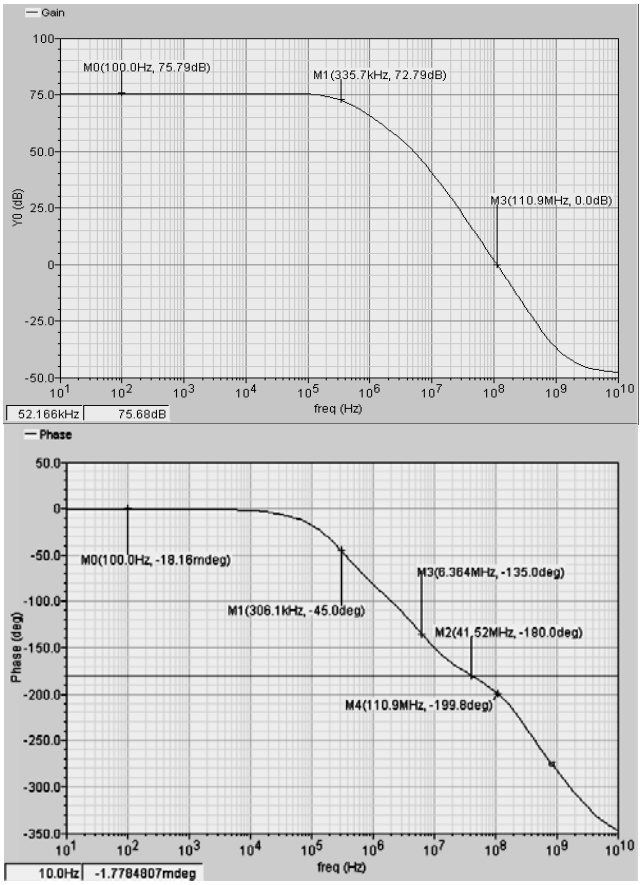

Fig. 3. Simulated transfer function of the op amp without compensation branch.

As op amp presented in this paper is intended for usage in mixed signal circuits, it needs to be able to suppress the interferences. For an example, the interferences that occur in the power supply voltage due to fast switching rate of the digital components. Parameters that describe how well the op amp is immune to these problems are CMRR and PSRR parameters. Simulation results for these parameters are shown indirectly with the gain of the common mode and the power supply signal gain in Fig. 6 and 7 respectively.

The rest of the simulation results are presented in Table IV. The results are achieved for an integrated resistor with temperature coefficient of -5500 ppm/°C. Manufactured circuits usually use an off-chip resistor which provides smaller temperature variations and better performance.

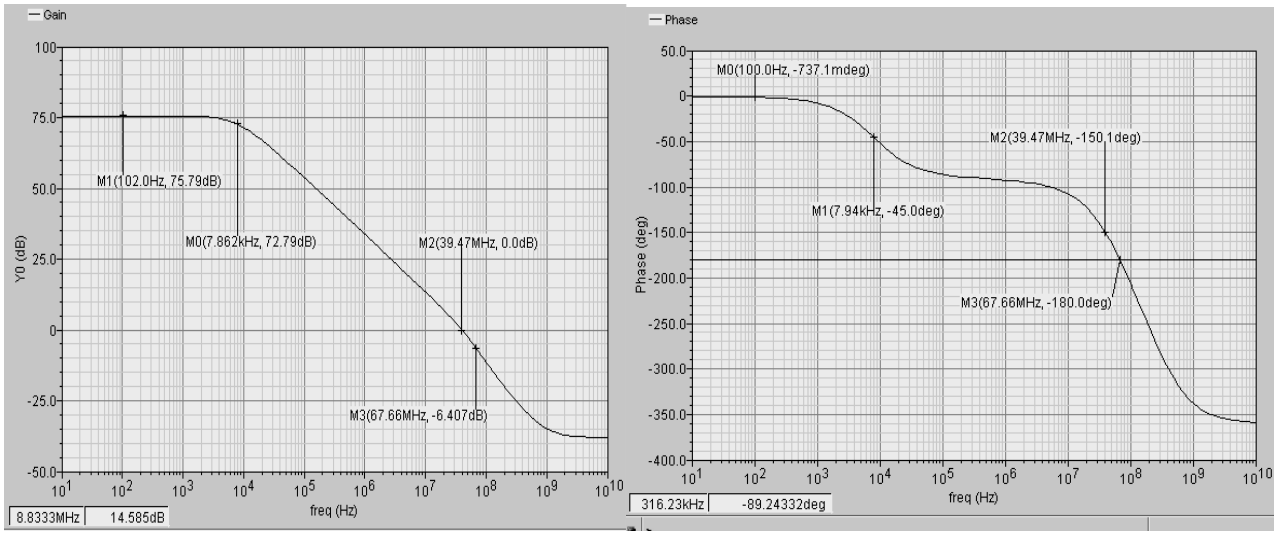

Fig. 4. Simulated transfer function of the op amp with just the Miler's capacitor C_C = 1.586 pF.

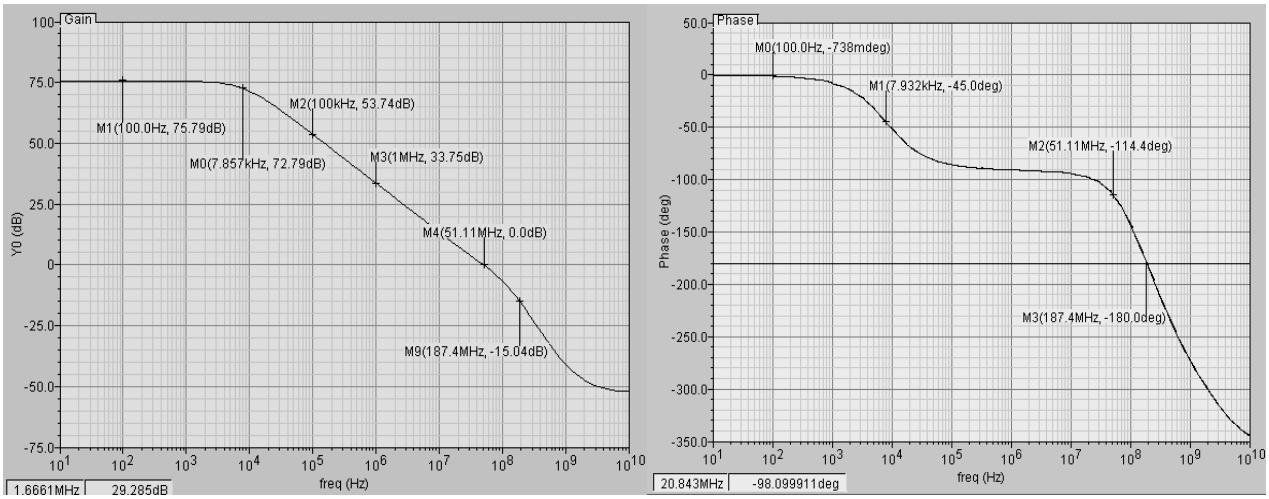

Fig. 5. Simulated transfer function of the op amp with the complete compensation branch.

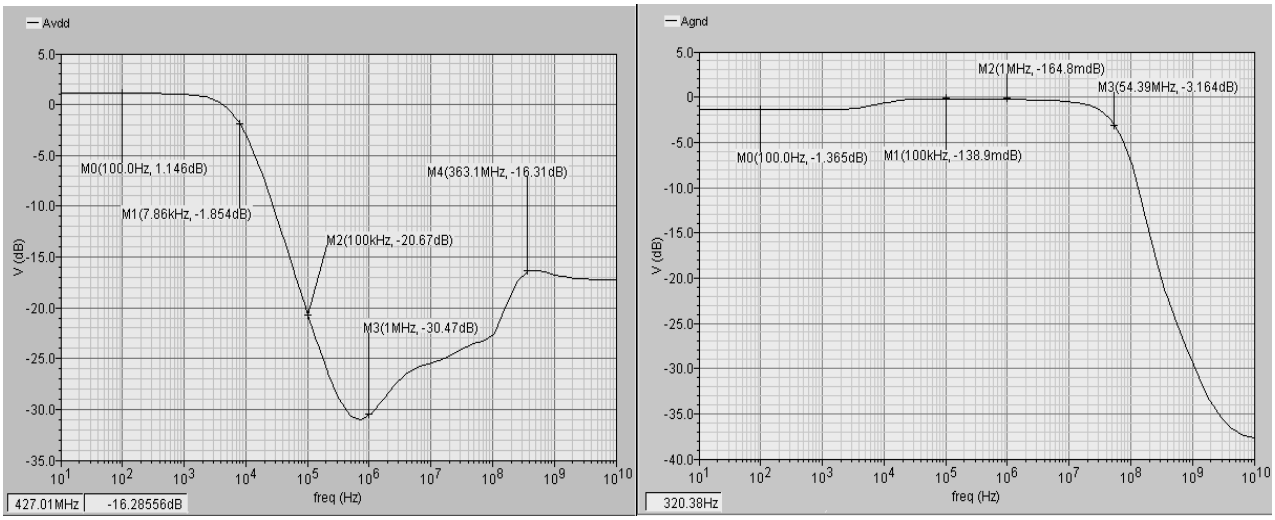

Fig. 6. Simulated results for the gain of a signal coming from VDD (left) and GND (right).

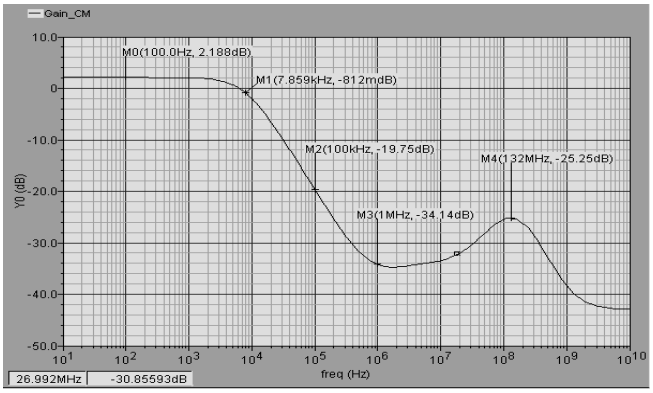

Fig. 7. Simulated results of the gain for a common mode signal at the input.

TABLE IV
SUMMARY OF ALL THE SIMULATION RESULTS

Parameter	Conditions	Min	Typ[(1)]	Max	Unit
Input CM	T=27°C,V_{DD}=1.8V	0	-	1	V
Output CM	T=27°C,V_{DD}=1.8V	0.32	-	1.34	V
Offset voltage	-40<T<125°C, 0.32<V_{INCM}<1V	-	0.06	0.11	mV
Phase margin	-40<T<125 °C, C_L=3pF	60	67	94[(2)]	°
Unity frequency	-40<T<125°C, C_L = 3pF,	42	52	117[(2)]	MHz
-3 dB bandwidth	T=27°C, C_L=3pF,	-	7.86	-	kHz
Slew rate	T=27°C,C_L=3 pF,	-	10	-	V/µs
Settling time	T=27°C,C_L=3 pF,	17[(4)]	-	150[(5)]	ns
Overshot	T=27°C,C_L=3 pF,	1.1[(4)]	-	13.7[(5)]	%
Linear range	T =27°C, C_L=3pF, V_{inCM}=550mV THD≤1%	- 2.2	- -	8 43.45	MHz mV
Diff. gain	-40<T<125°C	71	75	77	dB
CMRR	-40<T<125°C	63	73	94[(3)]	dB
PSRR	-40<T<125°C	63	74	78	dB
Supply current	-40< T<125°C	113	172	312	µA

(1) Typical values are for V_{CM}=V_{DD}/2, V_{DD} =1.8 V and T=27 °C.
(2) PM for the case when C_L = 0.
(3) CMRR for the case when V_{DD} + 10%.
(4) Linear settling time.
(5) Linear and nonlinear settling time.

IV. DISCUSSION

Several relationships between op amp parameters and its performance were noticed in the simulation results. First, the total gain and speed (unity frequency and slew rate) of the op amp show different behavior with the change of the supply current I_{DD}. With I_{DD} increase the output resistance decreases ($\sim 1/I_{DD}$) while the mosfet transconductance raises slower ($\sim\sqrt{I_{DD}}$) [3]. Increase in the overall gain, achieved with wider transistors, boosts parasitic capacitances. Consequently, the phase margin of the op amp is lowered. As its speed is directly proportional to the I_{DD}, change of supply current results in opposite gain and speed tendencies. It can be seen from the simulation results that the input and output common mode ranges have different tendency compared to the CMRR and PSRR parameters. High rejection parameters values require that transistors operate in deep saturation region. Therefore, higher drain-source voltages are needed which results in smaller common voltage range.

There are also a few limitations to the polarization circuit. For start, all transistors in the bias circuit need to be in saturation. In Fig. 1 there are, in either branch, two diode connected mosfets in series and as such their drain-source voltages will be at least equal to the threshold voltage. This doesn't leave much room for the source-gate voltages of pmos transistors and as a result current that they generate will be relatively small. Although negligible dissipation in the bias circuitry is one of the goals, extremely wide transistors for current generators (Q_5 and Q_6) are not an option. Additionally, the body effect of the nmos transistors consumes the already little voltage that you have at your disposal. Moreover, the drain potentials for Q_{10} and Q_{11} are not the same, which due to channel length modulation, results in different currents I_{D10} and I_{D11}.

The maximum capacitive load is 3 pF, which is too small if op amp is used as a discrete component. But if this op amp is used as a small part of a complex chip then this value is sufficient for driving the capacitive load of the next stage. Higher load at the output lowers the phase margin and makes the circuit more unstable because the second pole shifts to lower frequency Eq. (10) [2].

V. CONCLUSION

Design guidelines and simulation results for a two-stage CMOS operational amplifier were presented in this paper. Due to a delicate balance between parameters and the fact that op amp was designed in 150nm technology some compromise had to be made during the design. Targeted performance was accomplished for the specifications set and op amp can be used for low-voltage applications, consuming around 0.3 mW (V_{DD}=1.8V). Better temperature independency and wider operating temperature range (-40°C to 125°C) can be attained with a single off-chip resistor.

ACKNOWLEDGEMENT

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