Efficient Fault Effect Extraction for an Integrated Power Meter's ΣΔ ADC

Dejan Mirković, Dejan Stevanović and Vančo Litovski

Abstract - Analog to digital converter (ADC) is the vital part of many mixed-signal ICs because it interfaces analog signals from real world with digital logic on a chip. Errors made during conversion are hard to eliminate in the digital part that follows. Therefore, functional testing of ADC is a very important especially during developing of prototypes. Testing techniques for the ADC implemented in an integrated power-meter are considered first. A testing procedure based on efficient fault effect extraction will be proposed and implemented to a ΣΔ ADC. Encouraging results were observed.

Keywords – IMPEG, ΣΔ AD Converter**,** DFT, SC integrator

I. INTRODUCTION

Modern power meters are usually realized as solid state integrated SoC circuits. The functionality of this kind of circuits is based on acquiring instantaneous values of voltage and current. These values are obtained through some kind of analog-to-digital data conversion and further processed in digital domain. One such solution is realized as integrated circuit in LEDA laboratory and named IMPEG [1]. Basic block diagram of IMPEG chip is shown on Fig. 1.

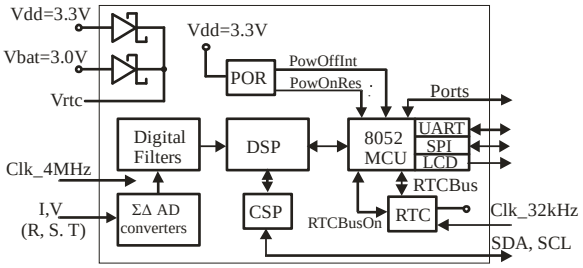

Fig. 1: IMPEG block diagram

From Fig. 1 one can notice the main functional blocks of IMPEG. One, in particular, block which is of prime concern of this paper, is ADC block. In the IMPEG solution ADC is realized as ΣΔ type of converter with second order noise shaping loop [2]. Since the accuracy of the ADC determines the quality of the power measurement, a proper function of this block is very important. So the ADC has to be fully tested.

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It is well known that time consumed for testing is the key parameter to be minimized from the manufacturing point of view. This fact holds primarily because the testing process increases time to market cost. In widely accepted automatic test equipment (ATE) testing of ADCs is based on the verification of a subset of converter performance parameters that include offset, gain, signal-to-noise ratio (*SNR*), total harmonic distortion (*THD*), integral nonlinearity (*INL*), differential nonlinearity (*DNL*) and power consumption. Dynamic performance parameters are estimated from FFT analysis performed over output bit stream. Static performance parameters can be determined from measured code transition edges (feedback loop test) or from the number of code occurrences in response to a periodic signal (histogram testing). The accuracy of such parameter measurements requires a large number of samples (approx. 16536 for 90 dB THD and *SNR* measurements) and up to 10 s of test time for a single channel 16-bit audio ADC.

There is a number of techniques and methods (e.g. built-in self-test (BIST)) for analog and mixed-signal circuitry in high resolution ADCs. All those techniques address the measurement of just one or of only a limited number of specification parameters using conventional techniques. One of such techniques that focus on minimization of test time and data required for FFT analysis is published in [3]. Often, most of these methods tends to require significant die area and dedicated additional test patterns for verification. In this paper a recent solution of design for testability (DFT) for ΣΔ ADC implemented in an integrated power meter is discussed [4].

This paper is organized as follows. The next section deals with different methods for ADC testing. After that we describe a practical way for testing the analog part of ΣΔ AD Converter. The paper concludes with important results obtained after testing the particular ΣΔ ADC.

II. ADC TESTING

Typical ADC tests are: ADC code edge measurement, DC tests, transfer curve tests, and dynamic ADC tests [5]. Each one of them will be briefly explained.

The aim of ADC code edge measurement is to find the input voltage threshold between two successive ADC codes that causes an output code to change. To measure the ADC linearity one needs to derive transfer curve of an ADC. Two well-known methods for transfer curve derivation are *center code testing* and *edge code testing* [4].

The center code testing gives artificially low DNL

value, and because of that this technique should be avoided. There are several different ways to search for the code edges. One of the most common techniques is the histogram method.

The simplest way to perform a histogram test is to apply a rising or falling linear ramp to the input of the ADC and collect samples from the ADC at constant sampling rate. The ADC samples are captured while the input ramp slowly moves from one end of the ADC conversion range to the other. The number of occurrences of each code is plotted as a histogram. It shows which codes are hit more often, indicating that they are wider codes. After obtaining the histogram, a code edge transfer curve must be derived using a mathematical equation that sums the code widths.

To compensate for the poor linearity of the ramp generators, the alternative, sinusoidal histogram method can be used. It is easier to produce a pure sinusoidal waveform than to produce a perfectly linear ramp. This method also allows testing in more dynamic, real-world situation, since ramps are varying very slowly. By using a sinusoidal signal instead of a ramp, one would expect to get more code hits at the upper and lower codes than at the center of the ADC transfer curve, even when testing a perfect ADC. The effects of the non-uniform voltage distribution can be removed after normalization.

DC Tests and Transfer Curve Tests comprise: DC Gain, DC offset, *INL*, *DNL*, monotonicity and missing codes tests. Once the ideal transfer curve has been established, DC gain and offset can be measured. The gain and offset are measured by calculating the slope and offset of the best-fit line.

Dynamic ADC parameters are: maximum sampling frequency, maximum conversion time, and minimum recovery time. More information about these parameters can be found in [5].

Considering all tests listed and an existing ADC architecture, it is very important to determine the significance and the feasibility of tests to be performed. Tests such as *INL* and *DNL* are not well suited for ΣΔ converters. Instead, channel tests like gain, offset, *SNR*, idle channel noise, etc., are commonly specified. When the resolution exceeds 12 or 13 bits, it becomes very expensive to perform transfer curve test such as *INL* and *DNL* because of the large number of code edges that must be measured. Fortunately, transmission parameters such as frequency response signal to distortion ratio (*SNDR*) and idle channel tests are much less time-consuming to measure.

III. Architecture of DFT for ΣΔ ADC

Simplified diagram of implemented DFT architecture for ΣΔ ADC is illustrated on Fig. 2. According to this diagram there are two test points available at the chip pins named *analog_out* and *digital_inout*. The pin *analog_out* provides access to two functionally important nodes of ADC's analog part. Practically it buffers multiplexed outputs of the first and the second integrator of ΣΔ modulator, respectively. The pin *digital_inout* represents bidirectional digital port which has dual role. Firstly, it provides access to the bit stream which represents coarsely quantized, oversampled value of analog input signal. Secondly through this pin the digital filters, that follow the ΣΔ modulator, can be fed with some externally generated bit sequence. So this pin enables implementation of testing algorithms weather for the whole ADC or just for the digital filters.

It is worth to mention that the converted value of analog input signal is stored in a 24 bit wide register which is refreshed with a rate of 4096 kHz. This register can be accessed using three wire serial communication port (SCP) at rate of 400 kHz. More about architecture illustrated in Fig. 2 can be found in [4] and [6].

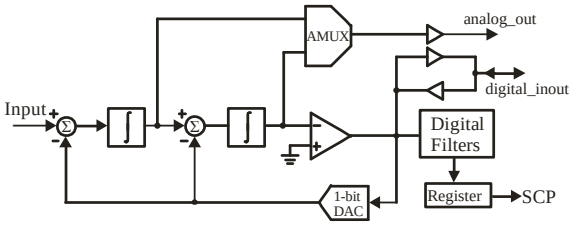

Fig. 2: DFT for ADC

In this section we dealt with the structure and operation of the implemented DFT architecture for ΣΔ ADC. This will help as to explain and establish a testing procedure for the analog part of ADC.

IV. Testing procedure for ΣΔ ADC

From earlier discussion in section one; one can conclude that ΣΔ ADC class of converters is most often characterized by dynamic parameters such as *SNR* or *SNDR*. Considering this fact the testing procedure presented in this paper adopts *SNR* and *THD* parameters as qualitative measure of ADC functionality. These parameters are extracted from FFT analysis of appropriate signal in one of previously discussed test points.

A. Test procedure

It is important to clarify that the proposed procedure is developed for the analog part of the ADC, namely ΣΔ modulator, and it is confirmed by means of simulation. Proposed testing procedure can be divided in several steps.

First, a test signal needs to be adopted. Because of the coarse quantizing, one bit, it is suitable to scan the output of the quantizer (*digital_inout* in Fig. 2) since there are only two values (logic zero or one). So this signal is measured (observed, simulated) for appropriate amount of time to get enough data for performing FFT. FFT analysis is preformed over collected set of data, and *SNR* and *THD* are estimated.

In order to create the fault dictionary, at this point, the previous steps should be repeated but with defects inserted

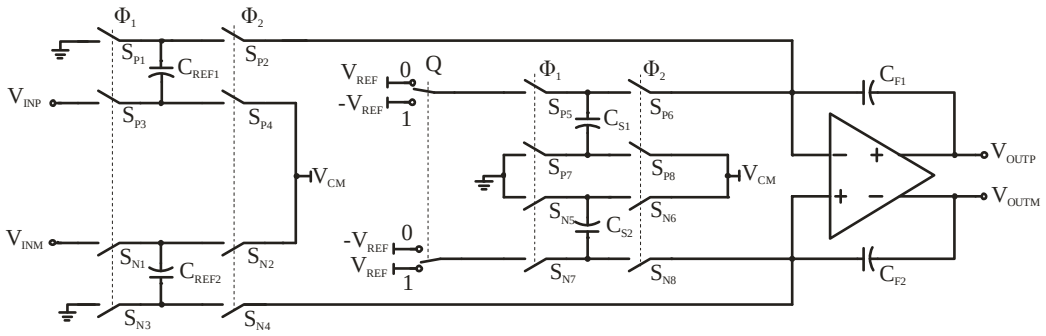

Fig. 3. Structure of the SC integrator in the sigma-delta modulator

in the analog part of the ΣΔ modulator (quantizer, SC integrator etc.). Single fault analysis is conceived. Finally, the responses of the fault-free and the faulty circuits are compared in order to establish testability for every inserted fault.

If there is deviation in *SNR* and/or *THD* values between the responses of the fault-free and the faulty circuit, the fault is covered with the test signal adopted in first step. Otherwise, the fault is masked so different test signal should be adopted, and the procedure repeated. Practically, the procedure is iteratively repeated until the given defect is covered i.e. appropriate test signal discovered. Besides *SNR* and *THD* parameters, visual inspection of the signal's spectrum can be helpful to detect presence of defect in the circuit.

Fortunately, because of the specificity of the circuit, every defect that forces any of the integrators, and the further quantizer, to saturate, will lead to malfunction. So sometimes is just enough to observe the waveform of the quantizer output. But when the effect of defect is not visible from output signal waveform then proposed testing procedure should be used.

B. Functionality of SC integrator

As it was mentioned in previous sections noise shaping is obtained with second order loop filter i.e. ΣΔ modulator. Each of two modulator stages is realized as SC, delaying, parasitic insensitive, integrator. The simplified, fully differential, realization of SC integrator is depicted in Fig. 3. Since the circuit is symmetrical to the horizontal axis for sake of simplicity one can concentrate on the top half of the circuit.

Every analog switch, S_{Ni}/S_{Pi}, where i= 1, ..,8, is realized as an NMOS transistor. The voltages V_{INP}, V_{OUTP} and V_{INM}, V_{OUTM} represent the input and output for a positive and negative analog signal, respectively. The port Q is the output of the quantizer while Φ_1 and Φ_2 are clock signal ports. The common mode voltage is denoted by V_{CM}, and the reference voltage with V_{REF}.

The operation of the SC integrator takes place in two non overlapping clock phases provided by Φ_1 and Φ_2. In the first phase, when the clock signal Φ_1 is active, the sampling capacitor (C_{S1}) is charged with charge that corresponds to instantaneous value of analog input signal, V_{INP}. In the second phase (Φ_2 active) the charge maintained on C_{S1} is transferred to the feedback capacitor C_{F1} and further to the output of the opamp, V_{OUTP}. Similarly, the charge proportional to $k \cdot V_{REF}$, where k is the ratio C_{REF1}/C_{F1}, is added to the feedback capacitor with plus or minus sign depending on the state of Q.

Knowing this, one can notice that the analog switch S_{P2}/S_{P4} (equivalently S_{N2}/S_{N4}) is vital for proper functioning of the SC integrator. During its activation charge is transferred to the output of the integrator. That was why malfunction of S_{P2} is picked to be tested with the proposed procedure. The testing procedure is applied to detect shorts and opens between all four transistor terminals (drain, gate, source and bulk) of the switch.

V. RESULTS

The proposed test procedure is applied on SPICE macro model of ΣΔ modulator which includes adequate MOS transistor model for 0.35 μm CMOS technology process. After simulation, FFT analysis, *SNR* and *THD* estimation are performed using appropriate MATLAB® script. All results are summarized in Table I.

The values for *THD* and *SNR* are given in homonymous columns. Column *detected* provides information weather defect is detected or not with the adopted excitation signal. The second row refers to the fault-free circuit, while the others represent faulty ones. The letters D, G, S, and B correspond to drain, gate, source, and bulk transistor terminals, respectively. Sine wave with 200mVpp magnitude and 50Hz frequency is adopted for excitation. After applying the test procedure to the circuit, this kind of excitation signal is shown to be adequate test signal for all defects in S_{P2}.

As can be seen from Table I all shorts between analog switch terminals, except gate-balk combination, result with malfunction of the circuit. So these defects could be detected only by observation of the waveform at the quantizer output. However, for gate-bulk short and drain, source and gate opens, the functionality of the circuit apparently stays unchanged. Because of that, presence of these defects cannot be detected by purely observing waveform of output signal.

TABLE I
SUMMARY OF RESULTS

			THD [%]	*SNR* [dB]	detected
Fault Free Circuit			0.067	78.53	-
Circuit with faults in S_{P2}	shorts	DS	98.742	-2.81	Yes
		GD	98.742	-2.81	Yes
		GS	98.741	-2.82	Yes
		DB	98.742	-2.81	Yes
		GB	5.11	57.9	Yes
		SB	98.742	-2.81	Yes
	opens	D	0.0204	86.13	Yes
		S	0.016	86.91	Yes
		G	0.028	85.79	Yes

So here is where proposed procedure pays its worth. For gate-bulk short there is a decrease of about 11dB in *SNR* and approximately 76 times increase in *THD* percentage.

For opens the effect is opposite as there are increases in *SNR* of about 8dB and approximately 3 times decreases in *THD* percentage.

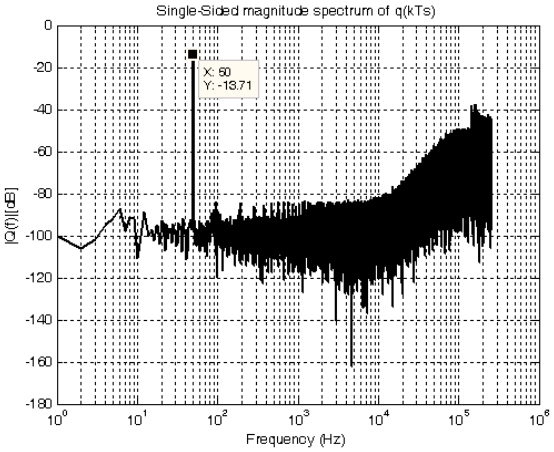

Fig. 4. Single-sided magnitude spectrum of fully functional circuit

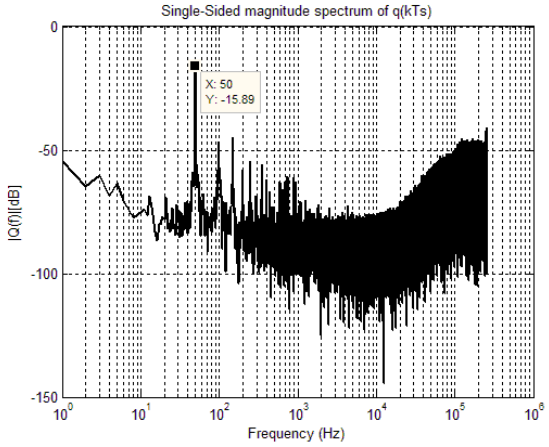

Fig. 5. Single-sided magnitude spectrum with shorted gate and bulk terminals of S_{P2} analog switch

As mentioned earlier, graphical representation of observed signal spectrum can be useful for defects detection. Fig. 4 illustrates single-sided magnitude spectrum of a quantizer output signal when there is no defect in circuit. From Fig. 4, single tone at 50Hz with -13.71dB magnitude can be noted. In band (below 2 kHz) noise floor is at about -100dB while out of band noise (over 2 kHz) is shaped with approximately 40dB/dec slope which corresponds to a second order modulator. For the sake of illustration on Fig. 5 single-sided spectrum of quantizer output whit presence of the S_{P2} gate-bulk (GB) defect in the circuit is shown. As one can notice from Fig. 5 the magnitude spectrum, along with *SNR* and *THD* parameters (see Table I), deviates from the spectrum of the fault-free circuit shown on Fig. 4.

VI. CONCLUSION

Review of standard test methods and principles which apply to mixed-signal data converter circuits is given. Some of the most popular ADC testing techniques are covered. Suitable parameters for functional verification of ΣΔ type of data converters are explained and adopted.

The architecture and functionality of the implemented DFT structure for integrated power meter ΣΔ ADC is commented. Appropriate test procedure for testing the analog part of ΣΔ ADC is developed and described along with the basic operation of the tested circuit. The test procedure is confirmed by means of SPICE simulation. Application of the proposed test procedure is presented through an example. Finally, the obtained simulation results are presented and commented.

ACKNOWLEDGEMENT

This research was partially funded by The Ministry of Education and Science of Republic of Serbia under contract No. TR32004

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