High level simulation of multiplexed incremental ADC for Integrated Power Meter

Dejan Mirković and Predrag Petković

Abstract – This paper presents an architectural solution for multiplexed ADC designed for a new generation of integrated power meter, IMPEG3. Basic problems related to the use of classic ΣΔ ADCs will be discussed. Proposed solution along with appropriate procedure for determining sampling frequency will be explained. High level simulation confirmed the developed behavioral model of the multiplexed ADC.

Keywords – Multiplexed ΣΔ ADC, behavioral modeling, integrated power meter.

I. INTRODUCTION

Contemporary power meters are based on integrated circuits dedicated to calculate energy using samples of current and voltage. Accuracy of these calculations is mainly determined by the quality and resolution of its analog frontend, namely analog-to-digital converter (ADC). The design team of LEDA laboratory at Faculty of Electronic Engineering, University of Niš continuously develops a series of own ASIC for electric power measuring applications. Fig. 1 shows the block diagram of the first version of a single-phase power meters (named IMPEG1) that has been prototyped in 2005. The analog frontend has been design as classic ΣΔ ADC.

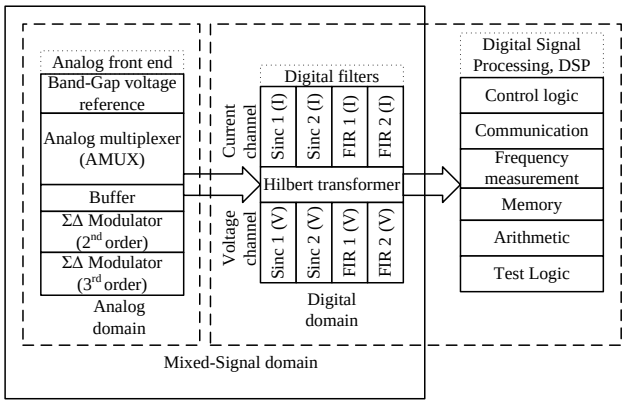

Fig. 1: Block diagram of IMPEG1 circuit

The prime purpose of ADC is to convert samples of current and voltage to digital domain. Conversion takes place in two separate channels for current and for voltage. The analog part of ADC consists of ΣΔ modulator [1].

Dejan Mirković and Predrag Petković are with the Department of Electronics, Faculty of Electronic Engineering, University of Niš, Aleksandra Medvedeva 14, 18000 Niš, Serbia, E-mail: {dejan, predrag}@elfak.ni.ac.rs.

Modulator serves to *shape* the noise generated during analog-to-digital signal discreatization. The nature of ΣΔ modulator is to operate with oversampled high frequency but with few number of output bits. IMPEG1 operates as single bit at output channel. Practically, the carrier of 50Hz is oversampled with 524288 Hz. The modulator suppresses HF noise out of the signal base band that has been limited to 2kHz. This implies noise rejection to high frequencies while the signal is processed with a low pass frequency (LP) filter. Integrators are used for LP filtering. The order of LP filters depends on needed ADC parameters. Signal to noise Ratio (SNR) and SFDR Spurious Free Dynamic Range (SFDR) are the most important input parameters in ADC design. They characterize the required resolution in terms of the number of output bits [1]. Initially the third order filter has been used for current and second order filter for voltage channel. However measurements on the prototyped samples have shown that the second order filtering is sufficient for both channels. In order to obtain multi-bit output one needs decimation digital filter. It accumulates the output signal with the oversampling frequency and provides wider digital word at the output at lower frequency. This word is a digital representation of instantaneous values of voltage and current, respectively.

The digital data is further fed into the Digital Signal Processing (DSP) block. DSP calculates RMS values of current and voltage, active power, reactive power, apparent power, corresponding energies, power factor (displacement factor) and frequency. This single-phase version of IMPEG chip is prototyped in CMOS 0.35 μm AMI Semiconductor technology.

The next generation of IMPEG solid-state power meters, named IMPEG2, was enhanced to fit for three-phase systems. Analog part of ADC was simply tripled for all three phases per channel. Therefore IMPEG2 was designed to have six ΣΔ modulators (three for currents and three for voltages of every phase). The digital part of the ADC has been redesign in a quite different manner comparing to IMPEG1. An original solution published in [2] describes the unique digital filter for processing of all three phases. Besides, IMPEG2 has been enhanced by other features mainly related to the digital part. The most important are embedded MCU8052, drivers for display and UART ports. More about these previous versions can be found at [3].

The subsequent generation of IMPEG required improvements in analog part.

The idea was to make compact ADC without lack of functionality. Consequently, an implicit solution was to

utilize multiplexed input that uses the same hardware. Some possible results for IMPEG3 were published in [4]. All of them considered separated current and voltage channel. This approach was motivated by different dynamic ranges and noise sensitivity. Fig. 2 depicts block diagram of the proposed ADC architecture.

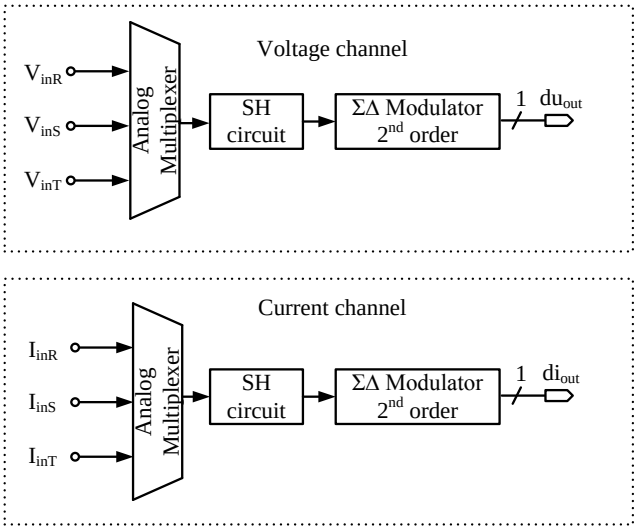

Fig. 2: Block diagram ADC in IMPEG3

In Fig. 2, V_{inR}, V_{inS} and V_{inT} represent analog line voltages while I_{inR}, I_{inS} and I_{inT} represent voltage equivalents of analog line currents (obtained with e.g. shunt resistors). Signals di_{out} and du_{out} denote one-bit ΣΔ modulator's outputs for voltage and current channels, respectively. Concept illustrated in Fig. 2 can be expanded to four inputs where the fourth port may be used for zero line current or for an external temperature sensor. The new version of IMPEG that is the subject of this paper will be designed to accept eight analog signals. This paper considers a new concept for multiplexed analog inputs. It relays on experiences obtained with the previous versions. Therefore, they will be shortly explained before we suggest a new architecture.

The next section describes different ADC architectures starting from ΣΔ modulator that has been used in previous IMPEG version. Thereafter the new architecture will be proposed together with procedure for determining fundamental operational parameter, namely sampling frequency, will be presented. It concludes with the subsection that elaborate stability of the proposed ΣΔ modulator architecture. The third and forth section describe the behavioral model and the corresponding results of simulation for the new ADC, respectively. The final section reviews conclusion remarks.

II. ARCHITECTURES OF ΣΔ MODULATOR

A. Previous architecture of ΣΔ modulator

Architecture of modulators built-in IMPEG1-3 ADC is CIFB (Cascade of Integrators Feed-Back) [1]. Fig. 3 shows block diagram of the second order ΣΔ modulator with CIFB architecture.

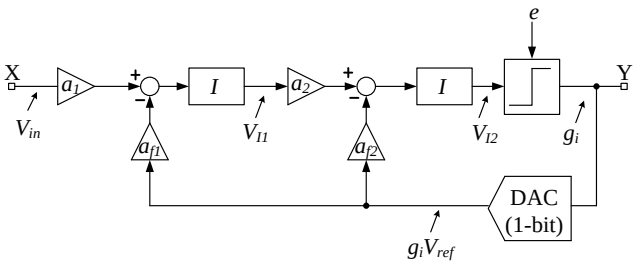

Fig. 3: Block diagram of 2nd order ΣΔ modulator with CIFB architecture

Blocks denoted with *I* represent DAI (Discrete Analog Integrators) with delay whose *Z* domain transfer function is given as:

$$I = \frac{z^{-1}}{1 - z^{-1}}, \tag{1}$$

where *z* is a complex variable. Input voltage is denoted with V_{in}, while V_{I1} and V_{I2}, represent the output of the first and the second integrator, respectively. Output of single-bit quantizer after i^{th} step is denoted with g_i. It can take values from set {1, -1}. Constants a_1, a_2, a_{f1} and a_{f2} are gains in direct path and feedback loops. The modulator is realized as Switched Capacitor (SC) circuit. More about architecture and realization of modulator shown on Fig. 3 can be found in [5].

Multiplexed implementation implies constant input signal during conversion of each channel. Therefore, the classic ΣΔ modulator architecture is not suitable for multiplexed application. Consequently, it is necessary to introduce a new architectural solution for ΣΔ modulator. In other words, classic ΣΔ type of ADC architecture is not favorable in combination with multiplexer on its input. The main problem with classic ΣΔ converter is too long settling time of digital part, i.e. digital filters that cause unacceptable delay between multiplexed channels. Therefore the architecture published in [6] is more suitable for multiplexing. This architecture is known as CIFF (Cascade of Integrators Feed-Forward) [7]. In order to be ready for accepting data from the new channel, ADC has to be reset after every conversion cycle. This implies that reset mast be introduced in ADC system. This kind of oversampling ADCs which contains resettable ΣΔ modulators are usually named *charge transfer*, *single shot* or *incremental* ADC [7].

B. Proposed architecture of ΣΔ modulator

Fig. 4 represents CIFF architecture of a second order ΣΔ modulator. Obviously, this architecture has only one feedback path from output (Y) to input (X), in contrast to CIFB architecture (Fig. 3) that has two. According to Fig. 3, blocks denoted with *I* represent DAI with *Z* domain transfer function given in (1).

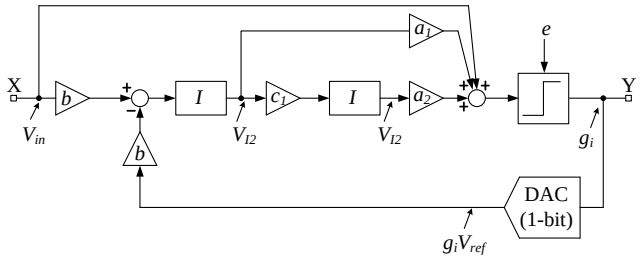

Fig. 4: Block diagram of 2nd order ΣΔ modulator with CIFF architecture

In Fig. 4 V_{in}, V_{I1} and V_{I2}, denotes input voltage and output voltage of the first and the second integrator, respectively. The output voltage of the single-bit DAC, denoted by term g_iV_{ref}, takes values $\pm V_{ref}$. Constants a_1, a_2, c_1 and b are modulator coefficients.

The modulator operates as follows.

Let suppose that the conversion of one input value requires n clock cycles. Each conversion starts from the initial state with $V_{I1}[0]= V_{I2}[0]= 0$V. The subsequent n outputs at the first integrator will take the following values:

$$\begin{aligned}
&V_{I1}[0] = 0\text{V}\\
&V_{I1}[1] = b\left(V_{in}[0] - g_0V_{ref}\right) + V_{I1}[0]\\
&V_{I1}[2] = b\left(V_{in}[1] - g_1V_{ref}\right) + V_{I1}[1]\\
&V_{I1}[2] = b\left(V_{in}[0] + V[1] - (g_{10} + g_1)V_{ref}\right),\\
&\vdots\\
&V_{I1}[n] = b\sum_{i=0}^{n-1}\left(V_{in}[i] - g_iV_{ref}\right)
\end{aligned} \qquad (2)$$

where $V_{in}[i]$ and $V_{I1}[i]$ stand for input analog voltage and the output voltage of the first integrator after i clock cycles, respectively while g_i denotes state of the quantizer after i^{th} cycle. Similarly, the output of the second integrator will be:

$$\begin{aligned}
&V_{I2}[0] = 0\text{V}\\
&V_{I2}[1] = c_1V_{I1}[0] + V_{I1}[0]\\
&V_{I2}[2] = c_1V_{I1}[1] + V_{I2}[1] =\\
&\qquad c_1\left(V_{I1}[0] + V_{I2}[1]\right)\\
&V_{I2}[3] = c_1V_{I1}[2] + V_{I2}[2] =\\
&\qquad c_1\left(V_{I1}[0] + V_{I1}[1] + V_{I2}[2]\right)\\
&\vdots\\
&V_{I2}[n] = c_1\sum_{j=0}^{n-1}V_{I1}[j] = c_1b\sum_{j=0}^{n-1}\sum_{i=0}^{j-1}\left(V_{in}[i] - g_iV_{ref}\right)
\end{aligned} \qquad ,(3)$$

where $V_{I2}[j]$ is output voltage of the second integrator after j^{th} clock cycle. This voltage takes value in range $\pm V_{ref}$.

$$-V_{ref} < V_{I2}[j] < +V_{ref}\,. \qquad (4)$$

During the conversion, SH circuit provides constant analog input signal $V_{in}[j] = V_{in0}$, for j=1,...,n. Therefore its contribution to the total sum in (4) is:

$$\sum_{j=0}^{n-1}\sum_{i=0}^{j-1}V_{in}[i] = \sum_{j=0}^{n-1}\sum_{i=0}^{j-1}V_{in0} = \binom{n}{2}V_{in0} = \frac{n(n-1)}{2!}V_{in0}\,. \qquad (5)$$

Substitution of (3) and (5) into (4) provides important result given in (6).

$$-\frac{V_{ref}}{c_1b}\frac{2!}{n(n-1)} < V_{in0} - \sum_{j=0}^{n-1}\sum_{i=0}^{j-1}g_iV_{ref} < +\frac{V_{ref}}{c_1b}\frac{2!}{n(n-1)}\,. \qquad (6)$$

The middle term of (6) represents the difference between analog input and the converted digital signal. Practically, it stands for conversion error that is bounded with $\pm$ (1/2)·V_{LSB}, where V_{LSB} is the analog voltage equivalent of the least significant bit. Therefore, it is defined as:

$$V_{LSB} = \frac{V_{ref}}{c_1b}\frac{2\cdot 2!}{n(n-1)}\,. \qquad (7)$$

Resolution of the converter can be expressed as:

$$\begin{aligned}
n_{bit} = \log_2\left(\frac{V_{in\max}}{V_{LSB}}\right) =\\
\log_2\left(n(n-1)\right) + \log_2\left(c_1b\right) + \,,\\
\log_2\left(\frac{V_{in\max}}{V_{ref}}\right) - 2
\end{aligned} \qquad (8)$$

where, n_{bit} is a number of bits. Assuming $n \gg 1$ one gets:

$$n_{bit} \approx 2\cdot\log_2 n + \log_2\left(c_1b\right) + \log_2\left(\frac{V_{in\max}}{V_{ref}}\right) - 2\,. \qquad (9)$$

For the full dynamic range of the input signal of $V_{inmax} = +V_{ref} - (-V_{ref}) = 2\cdot V_{ref,}$ and for normalized architecture (all modulator's coefficients equal to one) the resolution is reduced to:

$$n_{bit} \approx 2\cdot\log_2 n - 1\,. \qquad (10)$$

Expressions given in (9) or (10) allow calculation of the minimum number of clock cycles, n, needed to obtain n_{bit} resolution. Supposing that the required dynamic range is 96bB (knowing that each bit gives 6dB) it is easy to find that n_{bit} = 96/6 = 16 will met the request. According to (10) one easily calculates the minimum number of clock cycles to be n_{min} = 362. This means that the conversion of one channel lasts for 362 clock intervals. According to [7], in order to prevent saturation of integrators it is good practice to adopt $V_{inmax} \sim 0.67V_{ref}$ for second order modulator. Consequently, this increases the minimum number of clock cycles to n_{min} = 512. More information about evaluating n_{min} for higher order modulators can be found in [7].

So far the architecture and operation condition of the modulator has been determined. The next step is to define decimation filter that should average n_{min} bit stream to provide n_{bit} digital output. It is good practice to choose

filter to be at least one order higher than the modulator. Therefore this paper will consider a third order *Sinc* filter.

In general, transfer function of the L^{th} order *Sinc* filter expressed in z-domain is:

$$H(z)=\frac{1}{M^{L}}\left(\frac{1+z^{-M}}{1-z^{-1}}\right)^{L}, \qquad (11)$$

where $M= f_s/f_n$ is the oversampling ratio, f_n is Nyquist frequency defined as $f_n = 2\cdot BW$ and BW represents signal base band-width. In the particular case of IMPEG BW= 2048Hz. Realization of the *Sinc* filter is simplified if $M=2^K$, where K is an integer.

According to [7] procedure for determining sampling frequency should be:

1. For given n_{min} (n_{min}= 512) and adopted order of the modulator La (La = 2) determine the order of digital *Sinc* filter $L = La + 1$ (L= 3).
2. Increase n_{min} until obtain $M = n_{min}/L$ to be the first larger 2^K number. (M= n_{min}/L=512/3=170.667; the first larger 2^K is 256; choose M = 256 and recalculate $n_{min} = L\cdot M$=768).
3. Determine sampling frequency as $f_s=M\cdot f_n = M\cdot(2\cdot BW)$ ($f_s = 2^{20}$ Hz ≈ 2 MHz).

After n_{min} clock cycles filter will provide 16-bit digital word at the output. Therefore, one conversion cycle requires $n_{min}/f_s \approx 732.42\mu s$. The existing ΣΔ ADC in previous IMPEG versions provides digital data three times faster with 4096Hz rate, i.e. at every ~ 214.14μs. In order to maintain the same data rate towards digital part of the chip, a new three times higher sampling frequency is adopted ($f_{snew} = 3\cdot 2^{20}$ Hz ≈ 3.14 MHz). Eventually, the output of the digital filter provides 16-bit wide word after n_{min}/f_{snew} =1/4096s ~ 214.14μs.

Let consider a multiplexed ADC with N input signals (channels) based on architecture from Fig. 4. According to the fact that n_{min} depends on the required resolution (which was not the case with classic ΣΔ ADC), the multiplexing with the specified precision is feasible if $N\cdot n_{min}$ clock periods which fit within the available time window. In a case of IMPEG3, goal is to obtain N=4 conversions within the same time window of 214.14μs. This means that the 16-bit output word appears for all four channels with the rate of 4096Hz. Therefore the conversion time should be four times shorter for each channel and consequently, the new sampling frequency has to be N=4 times higher ($f_{sN}=N\cdot f_s$). After n_{min} clock periods, the obtained output of one channel is buffered, the whole converter (modulator and digital filter) is reset and another channel is fed to the input of ADC. This cycle repeats for all of N input channels. When N^{th} channel is converted, the buffered digital words are fed to DSP unit in parallel. The algorithm of conversion for N-channel multiplexed, incremental ADC contains the following steps:

1. First channel is selected with analog multiplexer.
2. With SH circuit selected signal is sampled and held for whole conversion cycle at the ADC's input.
3. After n_{min}/f_{sN} ($1/2^{14}$ s ≈ 61μs) digital output word is obtained and buffered for the selected channel; ADC is reset; and the subsequent new channel is selected from analog multiplexer to the ADC input.
4. Step 3 is repeated N times for all input channels.
5. After conversion of N^{th} channel; N n_{bit} -bit words are red with rate $f_{sN}/(n_{min}\cdot N)$ ($f_{sN}/(n_{min}\cdot N)$ = 4096 Hz); the procedure repeats from step 1.

One could conclude that due to the multiplexing a delay of n_{min}/f_{sN} = 61μs appears between each channel that could reflect on signal phase. Because the signal frequency is 50Hz, i.e. period 20ms, the delay is only about 0.3% of the signal's period. Therefore, the phase error is negligible. Nevertheless it is necessary to examine its influence on overall power and energy calculation. Obviously it is a systematic error that can be eliminated later in the digital part of the chip by the built-in programmable compensation.

C. Stability of proposed ΣΔ modulator architecture

So far the stability has not been considered. However it is an important feature of modulators. According to the common practice the stability will be appraised by analyzing the modulator behavior in *z*-domain. In ΣΔ convertors noise signal is fed back to the input and consequently it is responsible for stability. Therefore it is of important interest to analyze distributions of poles in Noise Transfer Function (*NTF*). *NTF* is defined as *Y*/*e* ratio and according to Fig. 4 the *NTF* can be written as:

$$NTF=\frac{z^2-2z+1}{(z-p_1)(z-p_2)}, \qquad (12)$$

where poles of the transfer function, p_1 and p_2, are related with modulator's coefficients as:

$$\begin{aligned} p_1+p_2 &= 2-a_1b \\ p_1p_2 &= 1+a_2c_1b-c_1b \end{aligned}. \qquad (13)$$

Obviously, the second order filter gives second order *NTF*. Modulator will be stabile if pair of *NTF* poles, p_1 and p_2, are placed inside the unit circle in z-plane. As mentioned earlier, for a second order modulator, it is good practice to limit integrator output voltages on $0.67V_{ref}$. The design task is to determine coefficient values that provide stabile and reliable operation. For adopted M=256, V_{Imax} = $0.67V_{ref}$ and maximum *NTF* out of band gain of 2, MATLAB® *Delta-Sigma Toolbox* [8] a value of $p_{1/2}$ = 0.3819 ± j·0.3004. Mapping these poles on CIFF architecture resulted in following coefficients: b = 0.475, c_1= 0.598, a_1= 2.59, a_2 = 2.755.

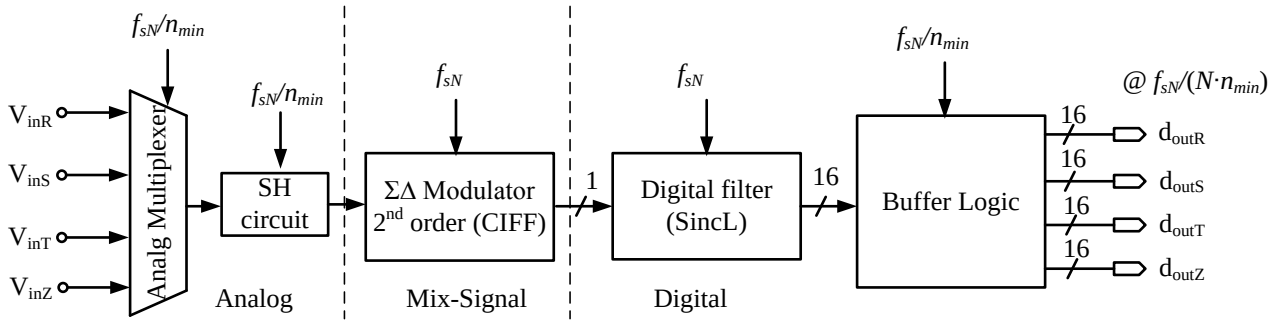

Fig. 5: Data flow block diagram of voltage channel ADC

Now, when all relevant design parameters of ΣΔ modulator and digital filter (f_s, *M*, *L*, *La*, *NTF* ...) are explained, behavioral model of ADC can be considered.

III. Modeling of ΣΔ Modulator

As Fig. 5 indicates, ADC is a mix-signal circuit. It can be roughly divided in three sub sections namely analog, mix-signal and digital. Analog block contain analog multiplexer and SH circuit. In this block signals are conditioned in analog domain i.e. can take any real value. Through the loop filters (integrators) signal is conditioned in the same manner i.e. in analog domain, while amount of the feedback is controlled digitally by quantizer and one-bit DAC outputs. Quantizer output is the point of connection between mix-signal and purely digital world. From this point signal is digitally processed and its value is constrained with two logic levels ("0" and "1").

Taking the previous in to account, behavioral model of proposed ADC architecture is developed. Model is built combining MATLAB®'s *Simulink* environment and appropriate scripts. The reset signal requires the use of time enabled and triggered *Simulink* blocks. These blocks provide a solid behavioral description of clock and reset dependent discrete system components. Therefore, DAI and digital filter/buffer logic registers are described in this manner.

All previously discussed characteristics of the proposed ADC architecture are built-in behavioral model. Obtained simulation results will be presented and commented in the subsequent sections.

IV. Simulation Results

The architecture of four inputs multiplexed, incremental ADC was verified on developed behavioral model. Sampling frequency is f_{sN} =12MHz (12582912Hz), while analog multiplexer, SH circuit and reset are clocked with f_{sN}/n_{min} =16384Hz (see Fig. 5). ADC is verified in presence of four sinusoidal signals with the same frequency of 50Hz and with amplitudes of 200mV, 100mV, 50mV and 25mV at inputs V_{inR}, V_{inS}, V_{inT} and V_{inZ}, respectively. Phases of V_{inR}, V_{inS}, and V_{inT} are shifted for for 120° while V_{inZ} have the same phase as V_{inR}. Fig. 6 illustrates waveforms of input and the output signals.

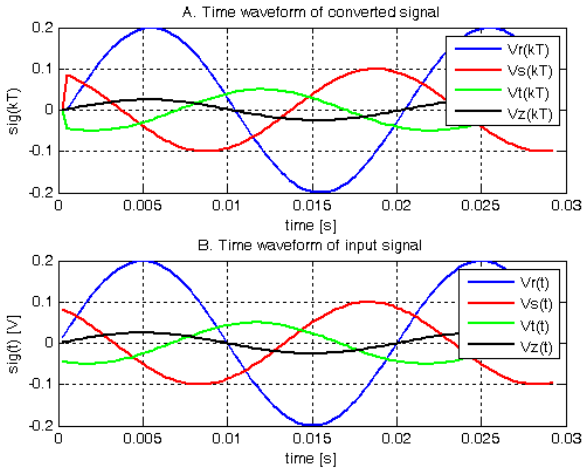

Fig. 6: Waveforms of input (A) and converted (B) signals of incremental ADC in voltage channel

The best insight into circuit behavior gives signal spectrum obtained by FFT analyzes over ADC's outputs. Fig. 7 illustrates the obtained results. Figure 7.a presents the complete, single-sided, signal spectrum up to the base band of 2kHz. Figure 7.b depicts magnified part of the spectra around 50Hz in order to clearly verify presence of all four signals. Obviously the obtained result confirms functionality of the proposed multiplexed, incremental, ADC architecture.

It should be mentioned that the current channel has identical architecture. Experience with previously prototyped IMPEG version suggests that the obtained SFDR better than 130dB at behavioral level have good chances to satisfy requested dynamic range of 80dB in current channel after fabrication.

V. Conclusion

One architectural solution for ADC that is going to be built-in integrated power meter, IMPEG3, suitable for multiplexed applications was presented in this paper. Review of the previous versions of IMPEG was given as well. The paper discussed some basic drawbacks of classic ΣΔ ADCs in multiplexing conditions. The central part of

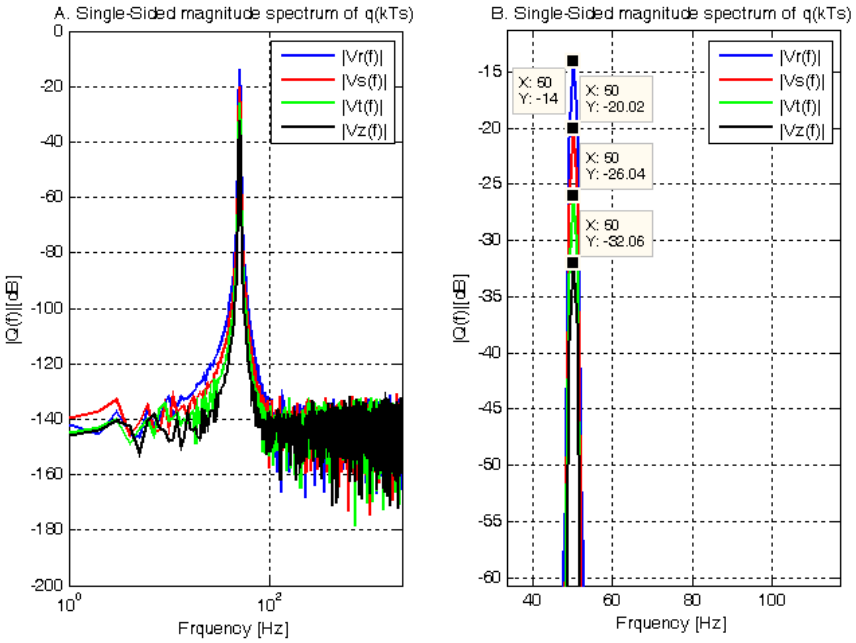

Fig. 7: One side magnitude spectrum of four channel ADC output (A) Full spectrum, logarithmic frequency scale; (B) Part of spectrum around 50Hz, linear frequency scale

this work proposed the new architecture with detailed derivation of mathematic expressions needed for behavioral modeling. In addition, the attention was paid to the appropriate algorithm for determining sampling frequency and to the stability criterion.

Basic modeling approaches are given. The developed behavioral model of the proposed architecture was confirmed by simulation using *Simulink*. The obtained simulation results are presented and commented.

Further research should consider other ΣΔ modulator and/or digital filter architectures. It has been shown in [7] that good results can be obtained with simpler digital filter architectures (e.g. cascade of two digital integrators), as well. Therefore, the expectation of better matched ADCs and reduced area comes through. Every, new, architecture should be well examined for design requirements in terms of dynamic range, resolution and noise sensitivity.

ACKNOWLEDGEMENT

This research was partially funded by The Ministry of Education and Science of Republic of Serbia under contract No. TR32004

REFERENCES

[1] R. Schreier, and G. C. Temes., "*Understanding Delta-Sigma Data Converters*", John Wiley & Sons, Inc., Hoboken, New Jersey, 2005.

[2] Marinković, M., „*Decimacioni filtri u trofaznom integrisanom meraču potrošnje električne energije*“, Magistarska teza, Univerzitet u Nišu, Elektronksi fakultet Niš, 2008. Ovde bolje da stavimo nešto na engleskom.ili

[2] Marinković, M., „*Decimation filters in tree-phase integrated power meters"*, Master Thesis, University of Niš, Faculty of Electronic Engineering, Nič, 2008. (In Serbian)

[3] http://leda.elfak.ni.ac.rs/projects/IMPEG/impeg.htm

[4] Mirković, D., Petković, P.: „*Multi channel Sigma-Delta A/D converter for integrated power meter*“, Proceedings of the Small Systems Simulation Symposium 2010, Niš, 12-14 February, 2010, pp. 90-93, ISBN 987-86-6125-006-4

[5] Nikolić, M., „Layout design of Mixed Signal CMOS Integrated Circuits“, Master Thesis, University of Niš, Faculty of Electronic Engineering, Nič, 2006. (In Serbian)

[6] C. Lyden, C. A. Ugarte, J. Kornblum, and F. M. Yung, "*Single shot sigma-delta analog-to-digital converter for multiplexed applications*" in *Proc. IEEE Custom Integrated Circuit Conf.*, Santa Clara, CA, May 1-4, 1995, pp. 203-206.

[7] J. Márkus, J. Silva, and G. C. Temes, "*Theory and applications of incremental delta-sigma converters*", IEEE Trans. Circuit Syst. I, Reg. Papers, vol. 51, no. 4, pp 678-690, Apr. 2004.

[8] R. Schreier. (2003) *The Delta–Sigma toolbox v6.0* (*Delsig*). Mathworks, Natick, MA. [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange