High level simulation of multiplexed incremental ADC for Integrated Power Meter

Dejan Mirković and Predrag Petković

Abstract – This paper presents an architectural solution for multiplexed ADC designed for a new generation of integrated power meter, IMPEG3. Basic problems related to the use of classic ΔΣ ADCs will be discussed. Proposed solution along with appropriate procedure for determining sampling frequency will be explained. High level simulation confirmed the developed behavioral model of the multiplexed ADC.

Keywords – Multiplexed ΔΣ ADC, behavioral modeling, integrated power meter.

I. INTRODUCTION

Contemporary power meters are based on integrated circuits dedicated to calculate energy using samples of current and voltage. Accuracy of these calculations is mainly determined by the quality and resolution of its analog frontend, namely analog-to-digital converter (ADC). The design team of LEDA laboratory at Faculty of Electronic Engineering, University of Niš continuously develops a series of own ASIC for electric power measuring applications. Fig. 1 shows the block diagram of the first version of a single-phase power meters (named IMPEG1) that has been prototyped in 2005. The analog frontend has been design as classic ΔΣ ADC.

Fig. 1: Block diagram of IMPEG1 circuit

The prime purpose of ADC is to convert samples of current and voltage to digital domain. Conversion takes place in two separate channels for current and for voltage. The analog part of ADC consists of ΔΣ modulator [1].

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Modulator serves to shape the noise generated during analog-to-digital signal discretization. The nature of ΔΣ modulator is to operate with oversampled high frequency but with few number of output bits. IMPEG1 operates as single bit at output channel. Practically, the carrier of 50Hz is oversampled with 524288 Hz. The modulator suppresses HF noise out of the signal base band that has been limited to 2kHz. This implies noise rejection to high frequencies while the signal is processed with a low pass frequency (LP) filter. Integrators are used for LP filtering. The order of LP filters depends on needed ADC parameters. Signal to noise Ratio (SNR) and SFDR Spurious Free Dynamic Range (SFDR) are the most important input parameters in ADC design. They characterize the required resolution in terms of the number of output bits [1]. Initially the third order filter has been used for current and second order filter for voltage channel. However measurements on the prototyped samples have shown that the second order filtering is sufficient for both channels. In order to obtain multi-bit output one needs decimation digital filter. It accumulates the output signal with the oversampling frequency and provides wider digital word at the output at lower frequency. This word is a digital representation of instantaneous values of voltage and current, respectively.

The digital data is further fed into the Digital Signal Processing (DSP) block. DSP calculates RMS values of current and voltage, active power, reactive power, apparent power, corresponding energies, power factor (displacement factor) and frequency. This single-phase version of IMPEG chip is prototyped in CMOS 0.35 μm AMI Semiconductor technology.

The next generation of IMPEG solid-state power meters, named IMPEG2, was enhanced to fit for three-phase systems. Analog part of ADC was simply tripled for all three phases per channel. Therefore IMPEG2 was designed to have six ΔΣ modulators (three for currents and three for voltages of every phase). The digital part of the ADC has been redesign in a quite different manner comparing to IMPEG1. An original solution published in [2] describes the unique digital filter for processing of all three phases. Besides, IMPEG2 has been enhanced by other features mainly related to the digital part. The most important are embedded MCU8052, drivers for display and UART ports. More about these previous versions can be found at [3].

The subsequent generation of IMPEG required improvements in analog part.

The idea was to make compact ADC without lack of functionality. Consequently, an implicit solution was to
utilize multiplexed input that uses the same hardware. Some possible results for IMPEG3 were published in [4]. All of them considered separated current and voltage channel. This approach was motivated by different dynamic ranges and noise sensitivity. Fig. 2 depicts block diagram of the proposed ADC architecture.

In Fig. 2, \( V_{inR}, V_{inS} \) and \( V_{inT} \) represent analog line voltages while \( I_{inR}, I_{inS} \) and \( I_{inT} \) represent analog line currents (obtained with e.g. shunt resistors). Signals \( d_{out} \) and \( d_{in} \) denote one-bit \( \Sigma \Delta \) modulator’s outputs for voltage and current channels, respectively. Concept illustrated in Fig. 2 can be expanded to four inputs where the fourth port may be used for zero line current or for an external temperature sensor. The new version of IMPEG that is the subject of this paper will be designed to accept eight analog signals. This paper considers a new concept for multiplexed analog inputs. It relays on experiences obtained with the previous versions. Therefore, they will be shortly explained before we suggest a new architecture.

The next section describes different ADC architectures starting from \( \Sigma \Delta \) modulator that has been used in previous IMPEG version. Thereafter the new architecture will be proposed together with procedure for determining fundamental operational parameter, namely sampling frequency, will be presented. It concludes with the subsection that elaborate stability of the proposed \( \Sigma \Delta \) modulator architecture. The third and forth section describe the behavioral model and the corresponding results of simulation for the new ADC, respectively. The final section reviews conclusion remarks.

II. ARCHITECTURES OF \( \Sigma \Delta \) MODULATOR

A. Previous architecture of \( \Sigma \Delta \) modulator

Architecture of modulators built-in IMPEG1-3 ADC is CIFB (Cascade of Integrators Feed-Back) [1]. Fig. 3 shows block diagram of the second order \( \Sigma \Delta \) modulator with CIFB architecture.

\[
I = \frac{z^{-1}}{1 - z^{-1}},
\]

where \( z \) is a complex variable. Input voltage is denoted with \( V_{in} \), while \( V_{ij} \) and \( V_{i2} \), represent the output of the first and the second integrator, respectively. Output of single-bit quantizer after \( i^{th} \) step is denoted with \( g_i \). It can take values from set \( \{1, -1\} \). Constants \( a_1, a_2, a_{ij} \) and \( a_{i2} \) are gains in direct path and feedback loops. The modulator is realized as Switched Capacitor (SC) circuit. More about architecture and realization of modulator shown on Fig. 3 can be found in [5].

Multiplexed implementation implies constant input signal during conversion of each channel. Therefore, the classic \( \Sigma \Delta \) modulator architecture is not suitable for multiplexed application. Consequently, it is necessary to introduce a new architectural solution for \( \Sigma \Delta \) modulator. In other words, classic \( \Sigma \Delta \) type of ADC architecture is not favorable in combination with multiplexer on its input. The main problem with classic \( \Sigma \Delta \) converter is too long settling time of digital part, i.e. digital filters that cause unacceptable delay between multiplexed channels. Therefore the architecture published in [6] is more suitable for multiplexing. This architecture is known as CIFF (Cascade of Integrators Feed-Forward) [7]. In order to be ready for accepting data from the new channel, ADC has to be reset after every conversion cycle. This implies that reset must be introduced in ADC system. This kind of oversampling ADCs which contains resettable \( \Sigma \Delta \) modulators are usually named charge transfer, single shot or incremental ADC [7].

B. Proposed architecture of \( \Sigma \Delta \) modulator

Fig. 4 represents CIFF architecture of a second order \( \Sigma \Delta \) modulator. Obviously, this architecture has only one feedback path from output (Y) to input (X), in contrast to CIFB architecture (Fig. 3) that has two. According to Fig. 3, blocks denoted with \( I \) represent DAI with \( Z \) domain transfer function given in (1).
In Fig. 4 $V_{in}$, $V_i$, and $V_{i2}$, denotes input voltage and output voltage of the first and the second integrator, respectively. The output voltage of the single-bit DAC, denoted by term $g_i V_{ref}$, takes values $\pm V_{ref}$. Constants $a_1$, $a_2$, $c_1$ and $b$ are modulator coefficients.

The modulator operates as follows.

Let suppose that the conversion of one input value requires $n$ clock cycles. Each conversion starts from the initial state with $V_{i1}[0]= V_{i2}[0]=0V$. The subsequent $n$ outputs at the first integrator will take the following values:

\[
V_{i1}[0] = 0V \\
V_{i1}[1] = b(V_{in}[0] - g_1 V_{ref}) + V_{i1}[0] \\
V_{i1}[2] = b(V_{in}[1] - g_1 V_{ref}) + V_{i1}[1] \\
V_{i1}[3] = b(V_{in}[0] + V_{in}[1] - (g_{10} + g_1) V_{ref}) , \tag{2}
\]

\[
V_{i1}[n] = b \sum_{i=0}^{n-1} V_{in}[i] - g_i V_{ref}
\]

where $V_{in}[i]$ and $V_{i1}[i]$ stand for input analog voltage and the output voltage of the first integrator after $i$ clock cycles, respectively while $g_i$ denotes state of the quantizer after $i$th cycle. Similarly, the output of the second integrator will be:

\[
V_{i2}[0] = 0V \\
V_{i2}[1] = c_1 V_{i1}[0] + V_{i1}[0] \\
V_{i2}[2] = c_1 V_{i1}[1] + V_{i1}[1] = c_1 (V_{i1}[0] + V_{i2}[1]) \\
V_{i2}[3] = c_1 V_{i1}[2] + V_{i1}[2] = c_1 (V_{i1}[0] + V_{i1}[1] + V_{i2}[2]) \\
V_{i2}[4] = c_1 V_{i1}[3] + V_{i1}[3] = c_1 (V_{i1}[0] + V_{i1}[1] + V_{i1}[2] + V_{i2}[3]) \tag{3}
\]

\[
V_{i2}[n] = c_1 \sum_{j=0}^{n-1} V_{i1}[j] = c_1 b \sum_{j=0}^{n-1} \sum_{i=0}^{g_i-1} V_{in}[i] - g_i V_{ref}
\]

where $V_{i2}[j]$ is output voltage of the second integrator after $j^{th}$ clock cycle. This voltage takes value in range $\pm V_{ref}$.

\[-V_{ref} < V_{i2}[j] < +V_{ref} . \tag{4}\]

During the conversion, SH circuit provides constant analog input signal $V_{in}[j] = V_{in}^{adj}$ for $j=1,...,n$. Therefore its contribution to the total sum in (4) is:

\[
\sum_{j=0}^{n-1} \sum_{i=0}^{g_i-1} V_{in}[i] = \frac{n}{2} \sum_{j=0}^{n-1} V_{in}[j] = \frac{n(n-1)}{2} V_{in}^{adj} . \tag{5}\]

Substitution of (3) and (5) into (4) provides important result given in (6).

\[-V_{ref} c_1 b n(n-1) < V_{in}^{adj} < +V_{ref} c_1 b n(n-1) . \tag{6}\]

The middle term of (6) represents the difference between analog input and the converted digital signal. Practically, it stands for conversion error that is bounded with $\pm (1/2) V_{LSB}$, where $V_{LSB}$ is the analog voltage equivalent of the least significant bit. Therefore, it is defined as:

\[
V_{LSB} = \frac{V_{ref} c_1 b}{n(n-1)} . \tag{7}\]

Resolution of the converter can be expressed as:

\[
n_{bit} = \log_2 \left( \frac{V_{in}^{max}}{V_{LSB}} \right) = 1 \log_2 (\frac{V_{in}^{max}}{V_{ref}}) + \log_2 (c_1 b) + , \tag{8}\]

\[
\log_2 \left( \frac{V_{in}^{max}}{V_{ref}} \right) > 2
\]

where, $n_{bit}$ is a number of bits. Assuming $n \gg 1$ one gets:

\[
n_{bit} \approx 2 \log_2 n + \log_2 (c_1 b) + \log_2 \left( \frac{V_{in}^{max}}{V_{ref}} \right) - 2 . \tag{9}\]

For the full dynamic range of the input signal of $V_{in}^{max} = +V_{ref} - (-V_{ref}) = 2V_{ref}$, and for normalized architecture (all modulator’s coefficients equal to one) the resolution is reduced to:

\[
n_{bit} \approx 2 \log_2 n - 1 . \tag{10}\]

Expressions given in (9) or (10) allow calculation of the minimum number of clock cycles, $n$, needed to obtain $n_{bit}$ resolution. Supposing that the required dynamic range is 96dB (knowing that each bit gives 6dB) it is easy to find that $n_{bit} = 96/6 = 16$ will met the request. According to (10) one easily calculates the minimum number of clock cycles to be $n_{min} = 362$. This means that the conversion of one channel lasts for 362 clock intervals. According to [7], in order to prevent saturation of integrators it is good practice to adopt $V_{in}^{max} \approx 0.67V_{ref}$ for second order modulator. Consequently, this increases the minimum number of clock cycles to $n_{min} = 512$. More information about evaluating $n_{min}$ for higher order modulators can be found in [7].

So far the architecture and operation condition of the modulator has been determined. The next step is to define decimation filter that should average $n_{bit}$ bit stream to provide $n_{bit}$ digital output. It is good practice to choose...
filter to be at least one order higher than the modulator. Therefore this paper will consider a third order Sinc filter.

In general, transfer function of the $L^{th}$ order Sinc filter expressed in z-domain is:

$$H(z) = \frac{1}{M^{L}} \left( \frac{1 + z^{-M}}{1 - z^{-1}} \right)^{L},$$

(11)

where $M = f_s/f_c$ is the oversampling ratio, $f_c$ is Nyquist frequency defined as $f_c = 2\cdot BW$ and $BW$ represents signal base-band-width. In the particular case of IMPEG $BW = 2048$Hz. Realization of the Sinc filter is simplified if $M = 2^K$, where $K$ is an integer.

According to [7] procedure for determining sampling frequency should be:

1. For given $n_{min}$ ($n_{min} = 512$) and adopted order of the modulator $La$ ($La = 2$) determine the order of digital Sinc filter $L = La + 1$ ($L = 3$).
2. Increase $n_{min}$ until obtain $M = n_{min}/L$ to be the first larger $2^K$ number. ($M = n_{min}/L = 512/3 = 170.667$; the first larger $2^K$ is 256; choose $M = 256$ and recalculate $n_{min} = L\cdot M = 768$).
3. Determine sampling frequency as $f_s = M\cdot f_n = M\cdot (2\cdot BW)$ ($f_s = 2^{20}$ Hz $\approx 2$ MHz).

After $n_{min}$ clock cycles filter will provide 16-bit digital word at the output. Therefore, one conversion cycle requires $n_{min}/f_s \approx 732.42$μs. The existing $\Sigma\Delta$ ADC in previous IMPEG versions provides digital data three times faster with 4096Hz rate, i.e. at every $\approx 214.14$μs. In order to maintain the same data rate towards digital part of the chip, a new three times higher sampling frequency is adopted ($f_{s\_new} = 3\cdot 2^{20}$ Hz $\approx 3.14$ MHz). Eventually, the output of the digital filter provides 16-bit wide word after $n_{min}/f_{s\_new} = 1/4096\mu s \approx 214.14$μs.

Let consider a multiplexed ADC with $N$ input signals (channels) based on architecture from Fig. 4. According to the fact that $n_{min}$ depends on the required resolution (which was not the case with classic $\Sigma\Delta$ ADC), the multiplexing with the specified precision is feasible if $N\cdot n_{min}$ clock periods which fit within the available time window. In a case of IMPEG3, goal is to obtain $N=4$ conversions within the same time window of 214.14μs. This means that the 16-bit output word appears for all four channels with the rate of 4096Hz. Therefore the conversion time should be four times shorter for each channel and consequently, the new sampling frequency has to be $N=4$ times higher ($f_{s\_new}/f_s = N/f_s$).

After $n_{min}$ clock periods, the obtained output of one channel is buffered, the whole converter (modulator and digital filter) is reset and another channel is fed to the input of ADC. This cycle repeats for all of $N$ input channels. When $N^{th}$ channel is converted, the buffered digital words are fed to DSP unit in parallel. The algorithm of conversion for $N$-channel multiplexed, incremental ADC contains the following steps:

1. First channel is selected with analog multiplexer.
2. With SH circuit selected signal is sampled and held for whole conversion cycle at the ADC’s input.
3. After $n_{min}/f_{s\_new}$ $(1/2^{14} \approx 61 \mu s)$ digital output word is obtained and buffered for the selected channel; ADC is reset; and the subsequent new channel is selected from analog multiplexer to the ADC input.
4. Step 3 is repeated $N$ times for all input channels.
5. After conversion of $N^{th}$ channel; $N\cdot n_{min}$-bit words are read with rate $f_{s\_new}/(n_{min} \cdot N)$ ($f_{s\_new}/(n_{min} \cdot N) = 4096$ Hz); the procedure repeats from step 1.

One could conclude that due to the multiplexing a delay of $n_{min}/f_{s\_new} = 61\mu s$ appears between each channel that could reflect on signal phase. Because the signal frequency is 50Hz, i.e. period 20ms, the delay is only about 0.3% of the signal’s period. Therefore, the phase error is negligible. Nevertheless it is necessary to examine its influence on overall power and energy calculation. Obviously it is a systematic error that can be eliminated later in the digital part of the chip by the built-in programmable compensation.

C. Stability of proposed $\Sigma\Delta$ modulator architecture

So far the stability has not been considered. However it is an important feature of modulators. According to the common practice the stability will be appraised by analyzing the modulator behavior in z-domain. In $\Sigma\Delta$ convertors noise signal is fed back to the input and consequently it is responsible for stability. Therefore it is of important interest to analyze distributions of poles in Noise Transfer Function (NTF). NTF is defined as $Y/e$ ratio and according to Fig. 4 the NTF can be written as:

$$\text{NTF} = \frac{z^2 - 2z + 1}{(z - p_1)(z - p_2)},$$

(12)

where poles of the transfer function, $p_1$ and $p_2$, are related with modulator’s coefficients as:

$$p_1 + p_2 = 2 - a_0b$$

$$p_1p_2 = 1 + a_1c_1b - c_0b.$$  

(13)

Obviously, the second order filter gives second order NTF. Modulator will be stable if pair of NTF poles, $p_1$ and $p_2$, are placed inside the unit circle in z-plane. As mentioned earlier, for a second order modulator, it is good practice to limit integrator output voltages on $0.67V_{\text{ref}}$. The design task is to determine coefficient values that provide stable and reliable operation. For adopted $M=256$, $V_{\text{max}} = 0.67V_{\text{ref}}$ and maximum NTF out of band gain of 2, MATLAB $\Delta$-Sigma Toolbox [8] a value of $p_{1/2} = 0.3819 \pm j0.3004$. Mapping these poles on CIFF architecture resulted in following coefficients: $b = 0.475$, $c_1 = 0.598$, $a_1 = 2.59$, $a_2 = 2.755$. 

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Now, when all relevant design parameters of $\Sigma\Delta$ modulator and digital filter ($f_s, M, L, La, NTF$ ...) are explained, behavioral model of ADC can be considered.

III. MODELING OF $\Sigma\Delta$ MODULATOR

As Fig. 5 indicates, ADC is a mix-signal circuit. It can be roughly divided in three sub sections namely analog, mix-signal and digital. Analog block contain analog multiplexer and SH circuit. In this block signals are conditioned in analog domain i.e. can take any real value. Through the loop filters (integrators) signal is conditioned in the same manner i.e. in analog domain, while amount of the feedback is controlled digitally by quantizer and one-bit DAC outputs. Quantizer output is the point of connection between mix-signal and purely digital world. From this point signal is digitally processed and its value is constrained with two logic levels (“0” and “1”).

Taking the previous into account, behavioral model of proposed ADC architecture is developed. Model is built combining MATLAB’s Simulink environment and appropriate scripts. The reset signal requires the use of time enabled and triggered Simulink blocks. These blocks provide a solid behavioral description of clock and reset dependent discrete system components. Therefore, DAI and digital filter/buffer logic registers are described in this manner.

All previously discussed characteristics of the proposed ADC architecture are built-in behavioral model. Obtained simulation results will be presented and commented in the subsequent sections.

IV. SIMULATION RESULTS

The architecture of four inputs multiplexed, incremental ADC was verified on developed behavioral model. Sampling frequency is $f_s = 12$ MHz (12582912Hz), while analog multiplexer, SH circuit and reset are clocked with $f_{SN/n_{min}} = 16384Hz$ (see Fig. 5). ADC is verified in presence of four sinusoidal signals with the same frequency of 50Hz and with amplitudes of 200mV, 100mV, 50mV and 25mV at inputs $V_{inR}$, $V_{inS}$, $V_{inT}$ and $V_{inZ}$, respectively. Phases of $V_{inR}$, $V_{inS}$ and $V_{inT}$ are shifted for for 120° while $V_{inZ}$ have the same phase as $V_{inR}$. Fig. 6 illustrates waveforms of input and the output signals.

![Fig. 6: Waveforms of input (A) and converted (B) signals of incremental ADC in voltage channel](image_url)

The best insight into circuit behavior gives signal spectrum obtained by FFT analyzes over ADC’s outputs. Fig. 7 illustrates the obtained results. Figure 7. a presents the complete, single-sided, signal spectrum up to the base band of 2kHz. Figure 7. b depicts magnified part of the spectra around 50Hz in order to clearly verify presence of all four signals. Obviously the obtained result confirms functionality of the proposed multiplexed, incremental, ADC architecture.

It should be mentioned that the current channel has identical architecture. Experience with previously prototyped IMPEG version suggests that the obtained SFDR better than 130dB at behavioral level have good chances to satisfy requested dynamic range of 80dB in current channel after fabrication.

V. CONCLUSION

One architectural solution for ADC that is going to be built-in integrated power meter, IMPEG3, suitable for multiplexed applications was presented in this paper. Review of the previous versions of IMPEG was given as well. The paper discussed some basic drawbacks of classic $\Sigma\Delta$ ADCs in multiplexing conditions. The central part of
this work proposed the new architecture with detailed derivation of mathematic expressions needed for behavioral modeling. In addition, the attention was paid to the appropriate algorithm for determining sampling frequency and to the stability criterion.

Basic modeling approaches are given. The developed behavioral model of the proposed architecture was confirmed by simulation using Simulink. The obtained simulation results are presented and commented.

Further research should consider other ΣΔ modulator and/or digital filter architectures. It has been shown in [7] that good results can be obtained with simpler digital filter architectures (e.g. cascade of two digital integrators), as well. Therefore, the expectation of better matched ADCs and reduced area comes through. Every, new, architecture should be well examined for design requirements in terms of dynamic range, resolution and noise sensitivity.

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REFERENCES


integrisanom meraču potrošnje električne energije”, Magistarska teza, Univerzitet u Nišu, Elektronski fakultet Niš, 2008. Ovde bolje da stavimo nešto na engleskom ili